## ABSTRACT OF THE DISCLOSURE

A delay circuit, e.g., for a semiconductor device, having a plurality of cascade-connected stages that successively delay an input signal, may include: plural cascaded-connected delay devices representing instances of a first type of delay unit corresponding to the stages, respectively; plural resistance units coupled between a node having a source voltage of varying magnitude Vvar and odd-numbered ones of the delay devices, respectively; and plural capacitance units coupled between a node having another voltage Vuni of substantially uniform magnitude relative to Vvar and nodes representing the outputs of the odd-numbered delay devices; where corresponding ones of the plurality of capacitor units and the plurality of resistance units represent instances, respectively, of a second type of delay unit.